JUELICH SUPERCOMPUTING CENTRE (JSC)

IXPUG conference 2019 @ CERN

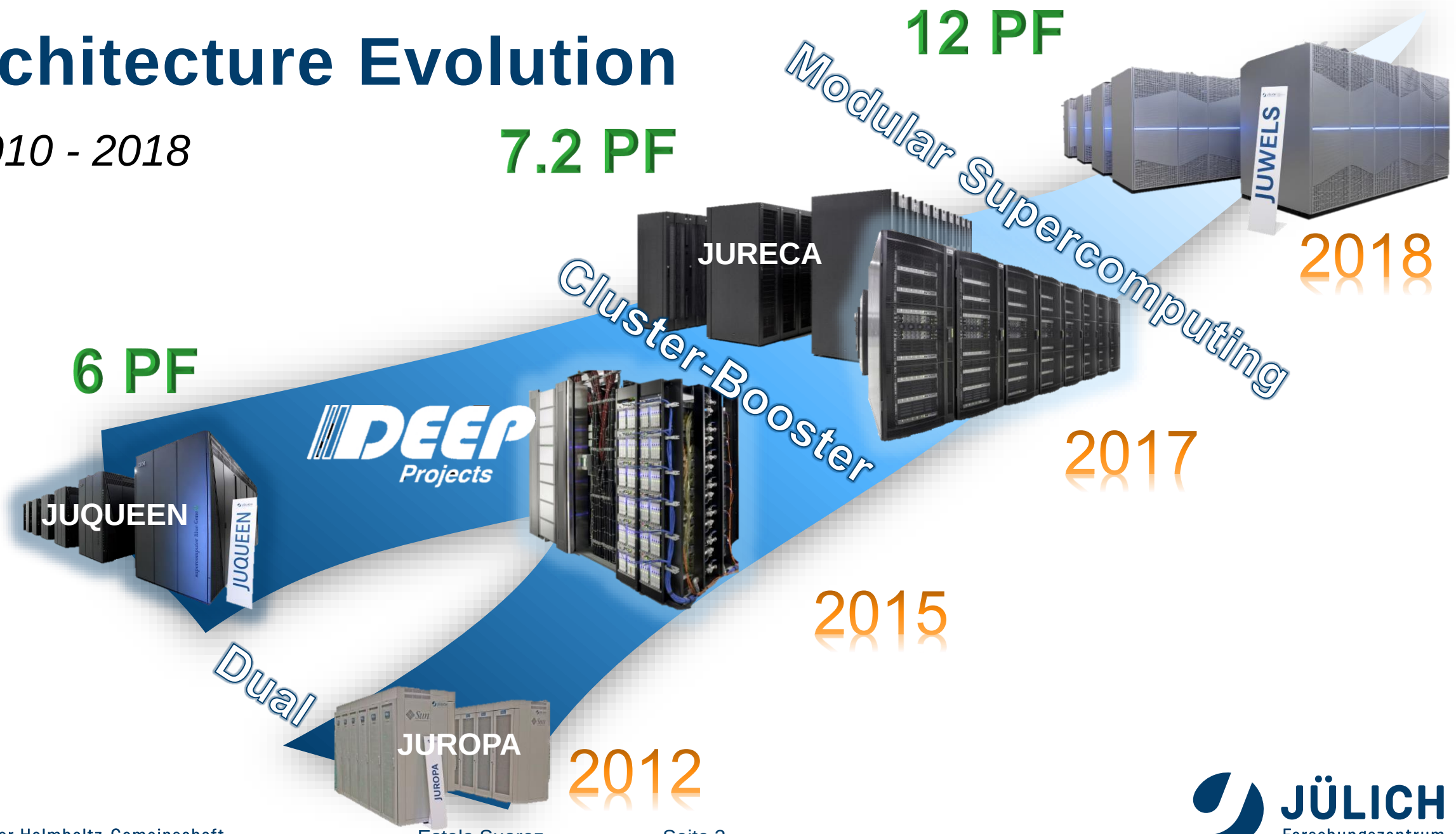
25.09.2019 | ESTELA SUAREZ

OUTLINE

- JSC from 2011 to 2018
  - Production systems
    - JURECA
    - JUWELS
  - Application fields
  - Support and Research
- Modular Supercomputing Architecture
  - Modular applications
  - DEEP-EST prototype

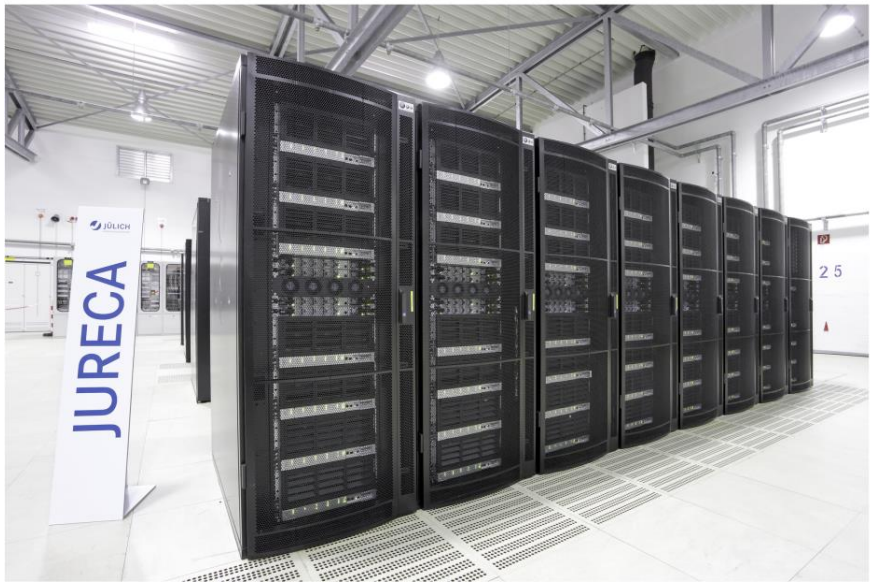
Architecture Evolution

2010 - 2018



JURECA

a) JURECA Cluster



b) JURECA Booster

Source: FZJ

	Cluster	Booster
Processor	Intel Xeon (Haswell)	Xeon Phi (KNL)
Interconnect	InfiniBand EDR	OmniPath
Node count	1,872	1,640
Peak Perf. (PFlops)	1,8 (CPU) + 0.4 (GPU)	5

JUWELS

a) JUWELS Cluster

Source: FZJ

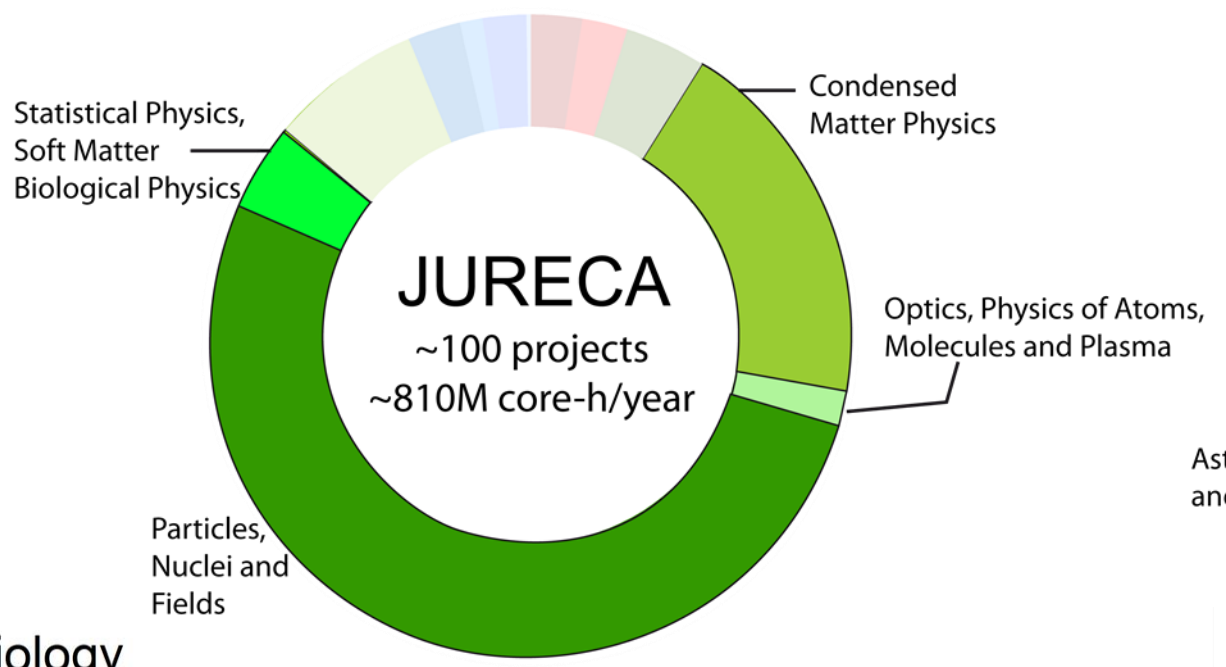
b) JUWELS Booster

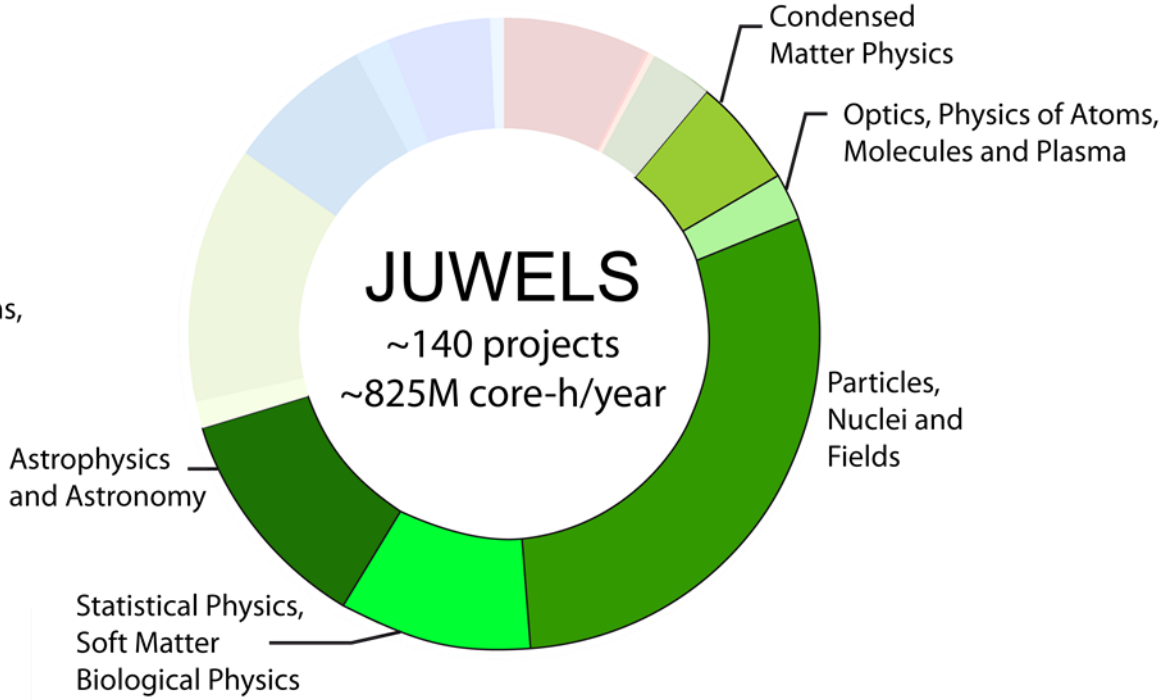
Installation in 2020

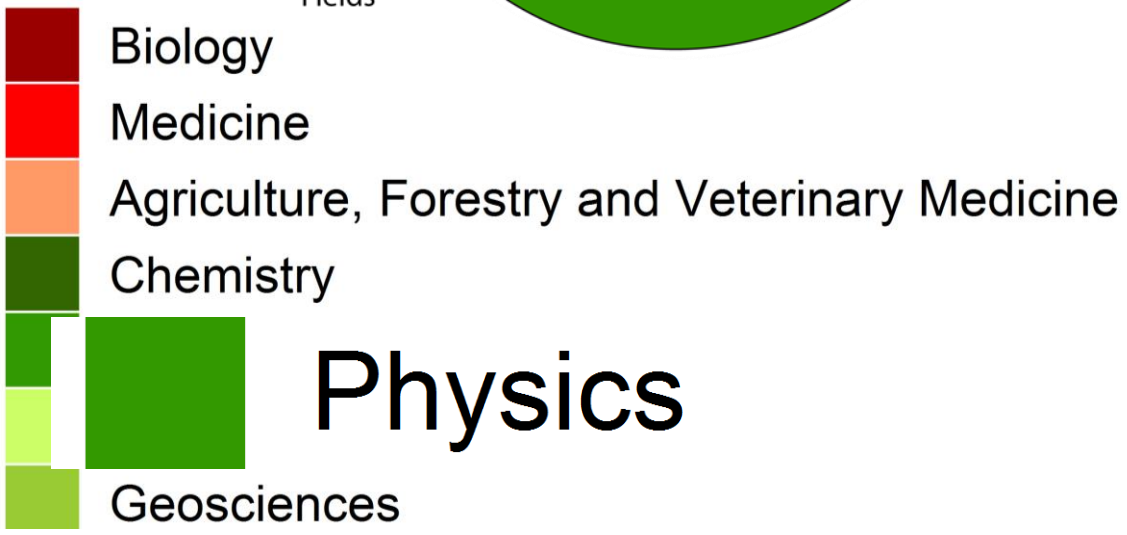
	Cluster	Booster
Processor	Intel Xeon (Skylake)	GPU-based
Interconnect	InfiniBand EDR	InfiniBand HDR
Node count	2,500	TBA
Peak Perf. (PFlops)	10,4 (CPU) + 1.6 (GPU)	>60 PFlop/s

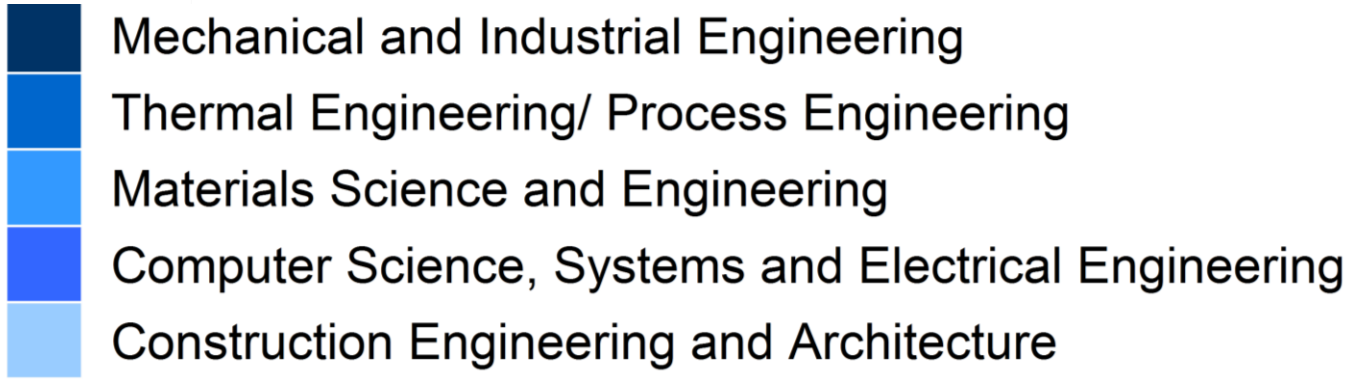
Application fields

Source: FZJ

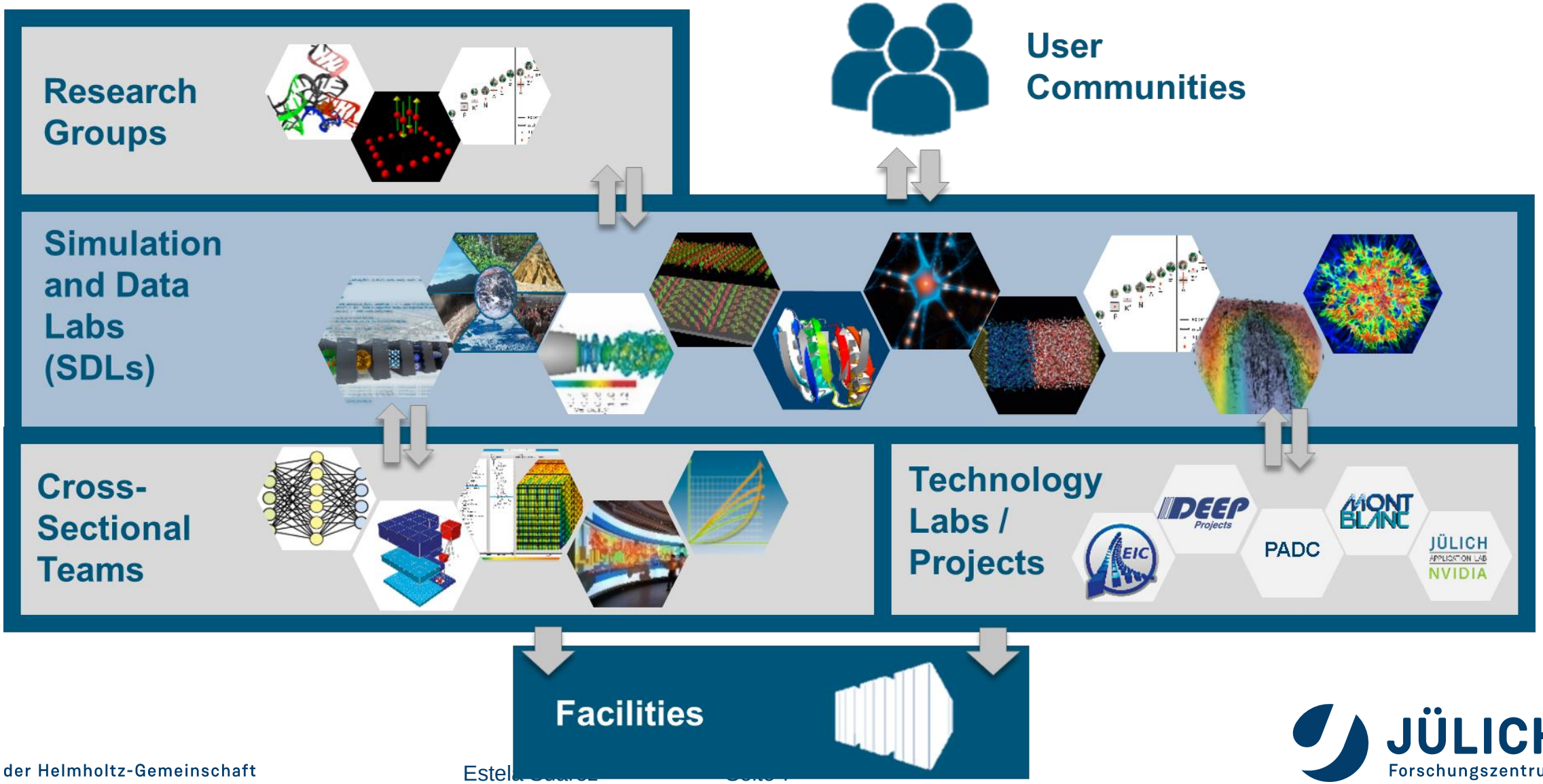








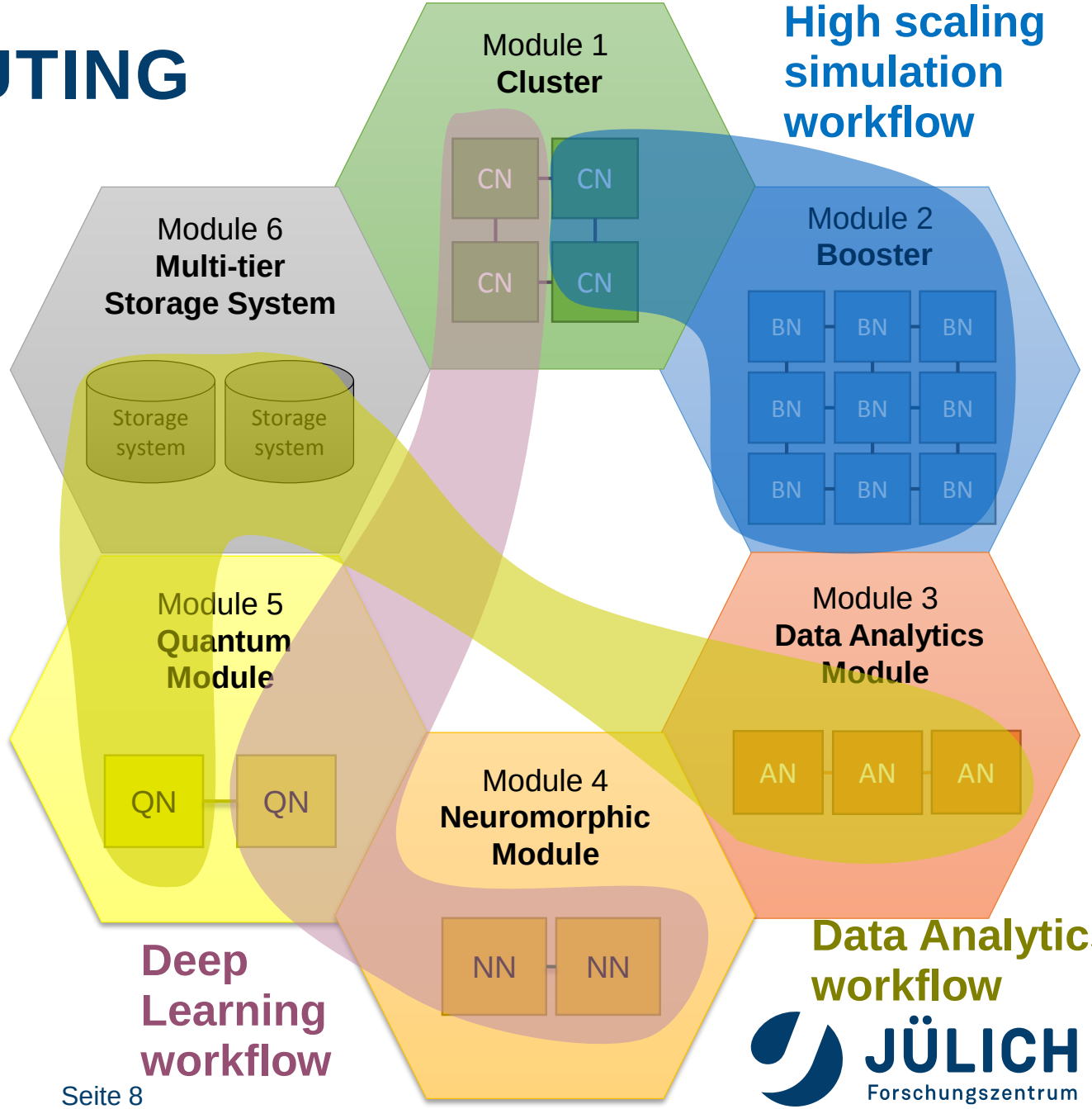
User Support and own Research



Source: FZJ

MODULAR SUPERCOMPUTING

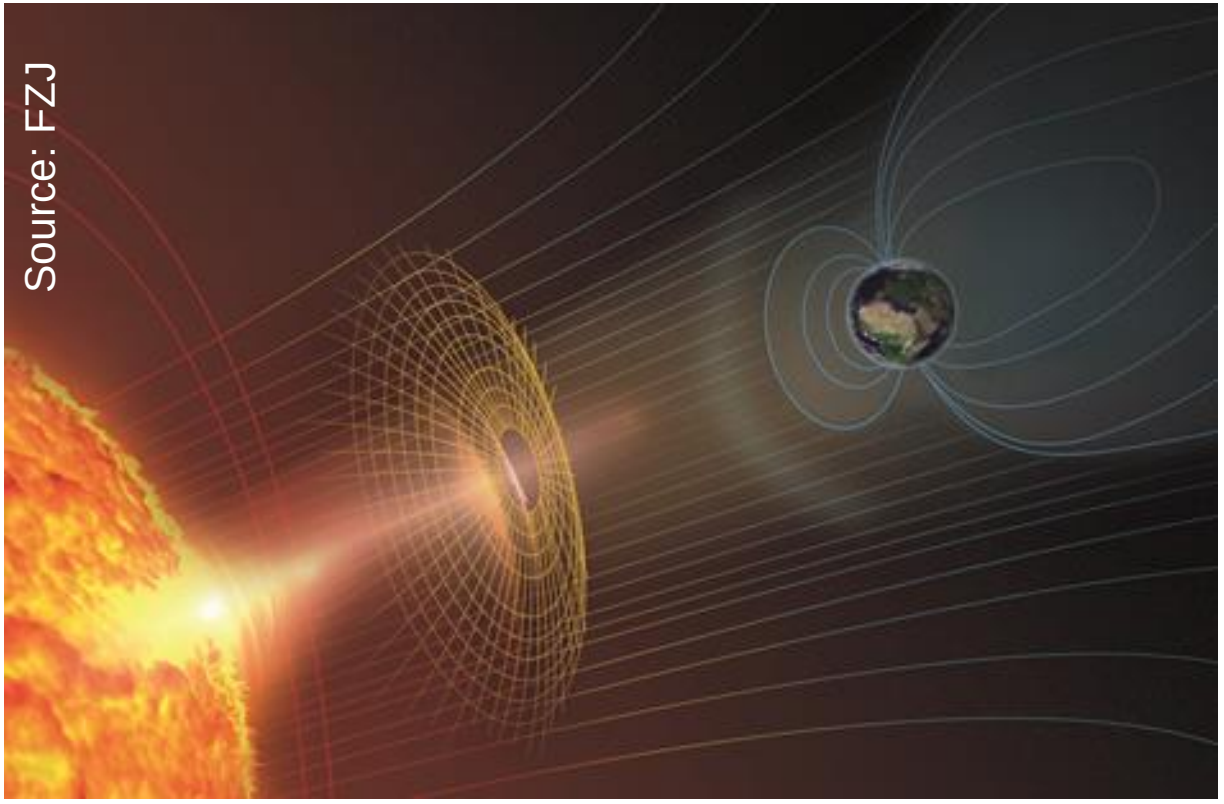
- **Composable resources**
  - Disaggregated: CPU, GPU, FPGA
  - Specific: quantum systems, neuromorphic devices
  - Interconnected
  - Unified Software environment
- **Advantages**
  - Fit diverse applications:
    - *HPC, Analytics, AI, Deep Learning*
  - Cost effective scaling
  - Effective resource sharing

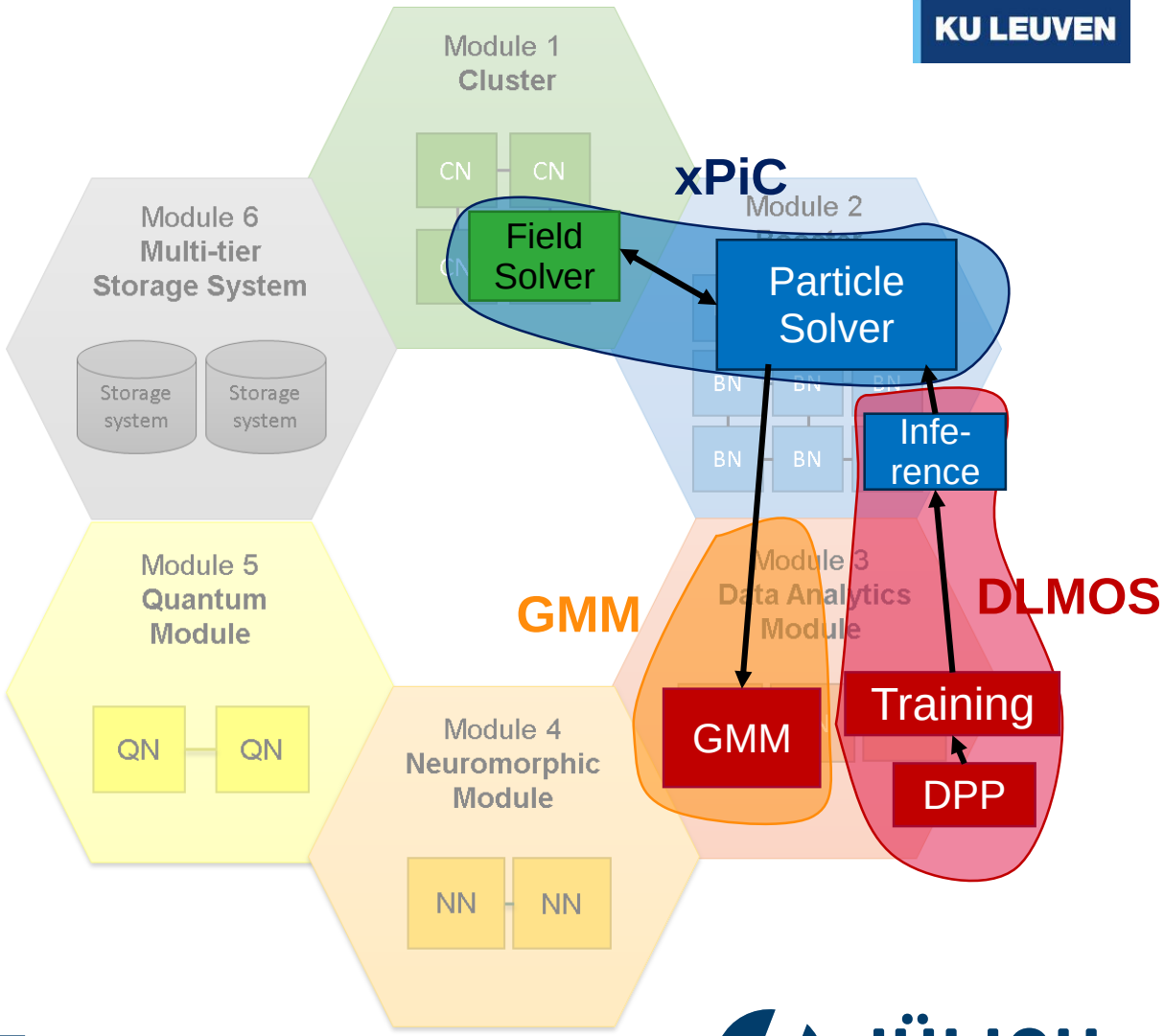


- **E. Suarez***, N. Eicker, Th. Lippert, "*Modular Supercomputing Architecture: from idea to production*", Chapter 9 in Contemporary High Performance Computing: from Petascale toward Exascale, Volume 3, pp 223-251, CRC Press. (2019)
- **E. Suarez***, N. Eicker, and Th. Lippert, *"Supercomputer Evolution at JSC"*, Proceedings of the 2018 NIC Symposium, Vol.49, p.1-12, (2018) [online: http://juser.fz-juelich.de/record/844072].

JÜLICH Forschungszentrum

xPiC – Mapping on a Modular Supercomputer

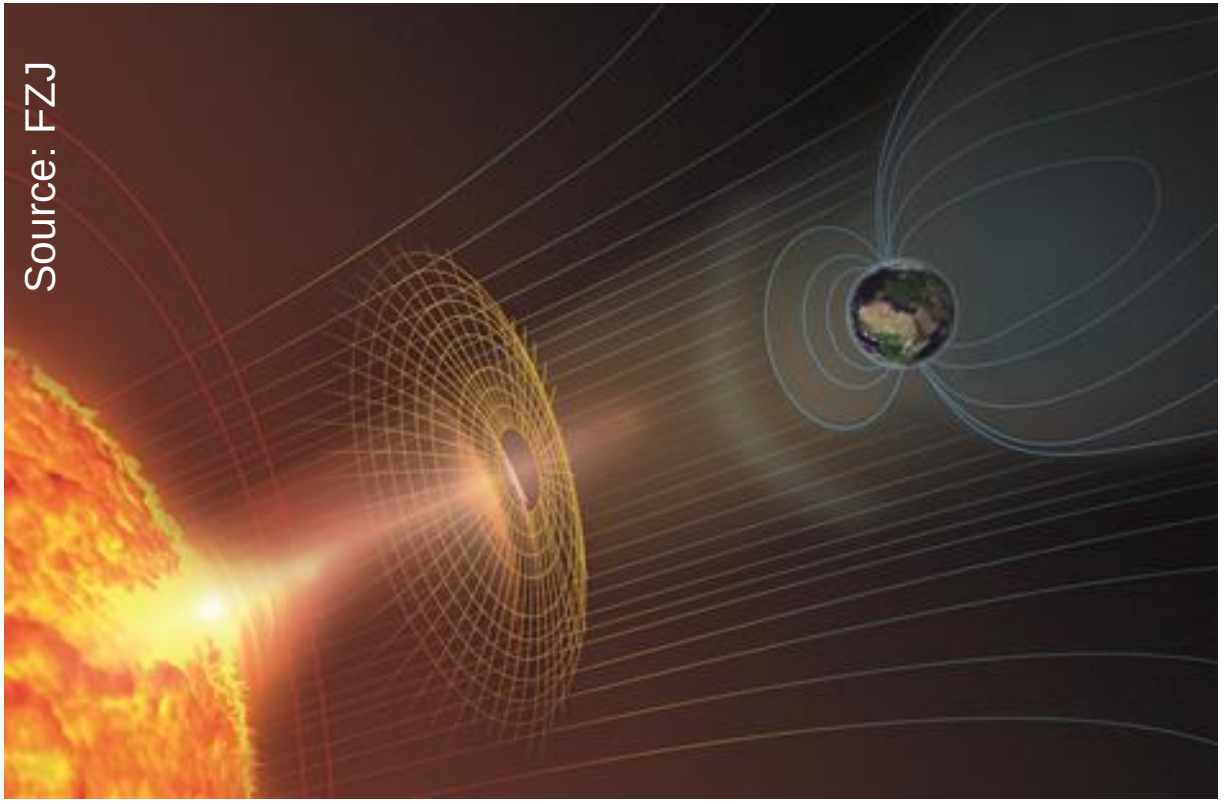


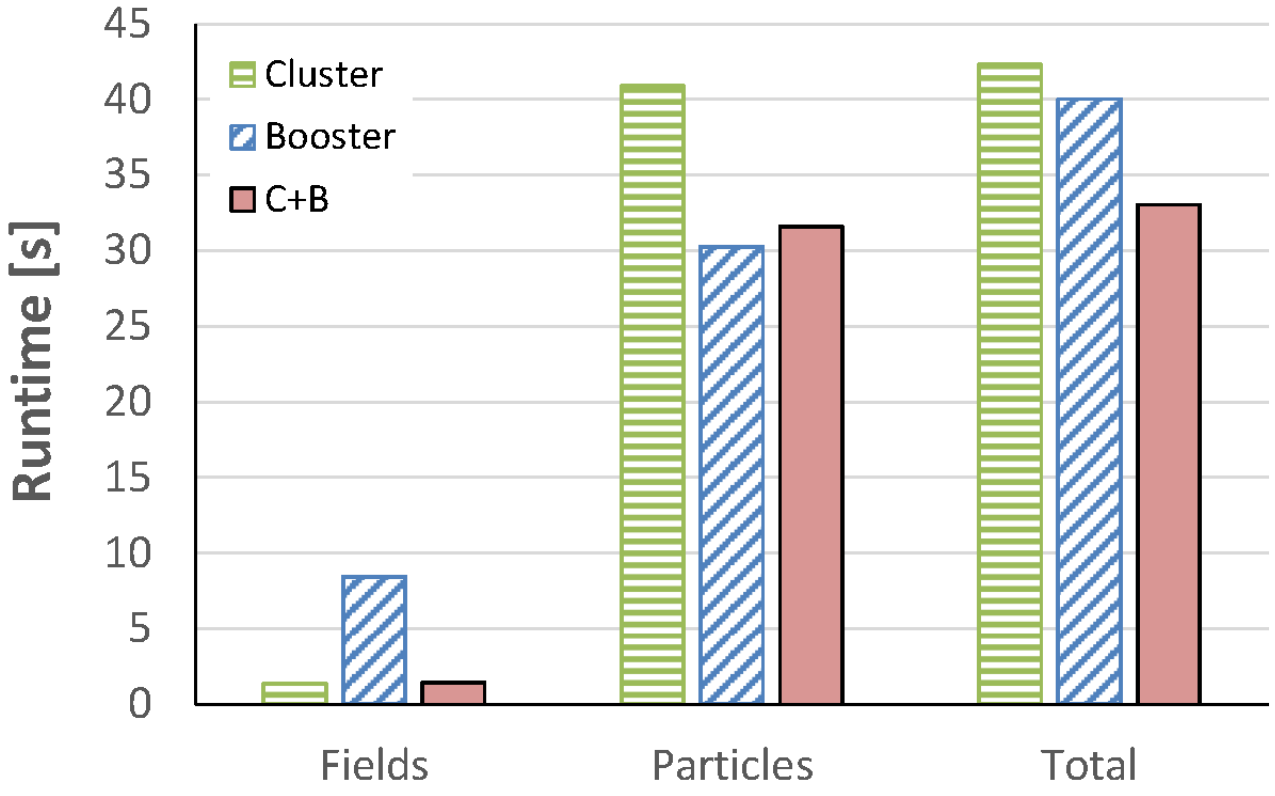


DLMOS ⟶ **xPiC** ⟷ **GMM**

A. Kreuzer, J. Amaya, N. Eicker, E. Suarez*, *"Application performance on a Cluster-Booster system"*, 2018 IPDPSW) HCW (20th International Heterogeneity in Computing Workshop), Vancouver (2018), p: 69 - 78. [doi: 10.1109/IPDPSW.2018.00019]

xPiC – Mapping on a Modular Supercomputer



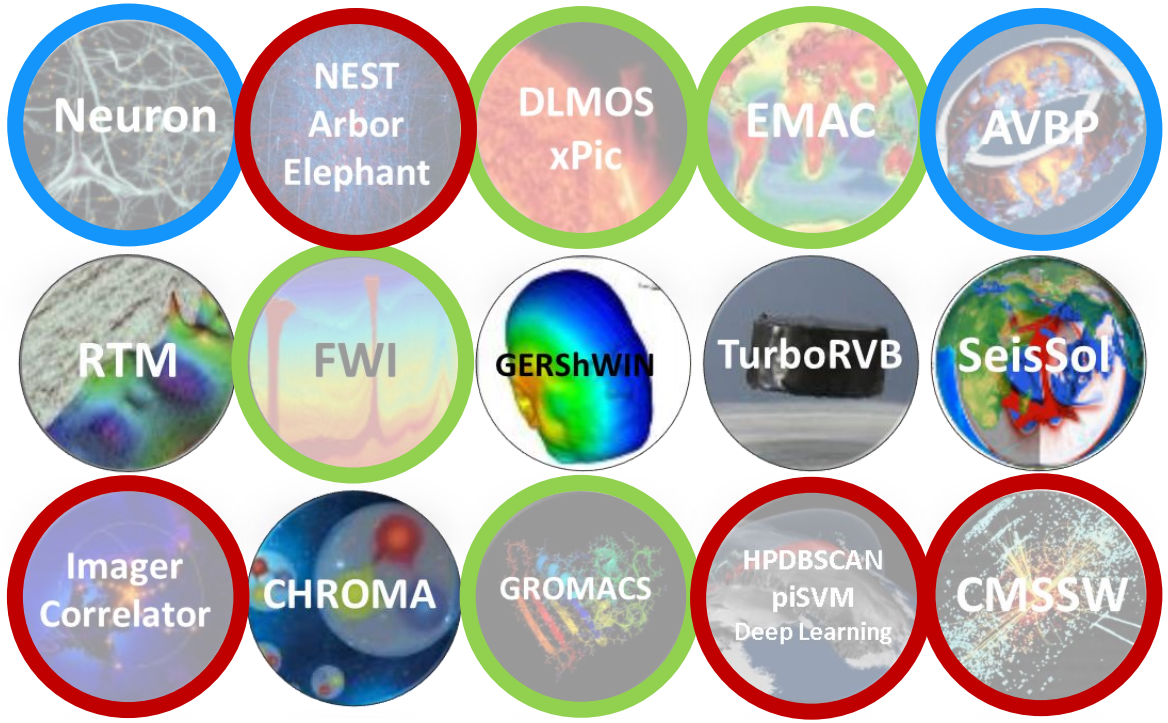


DLMOS ⟶ **xPiC**

1× node → 25% gain
8× nodes → 35% gain

A. Kreuzer, J. Amaya, N. Eicker, E. Suarez*, *"Application performance on a Cluster-Booster system"*, 2018 IPDPSW) HCW (20th International Heterogeneity in Computing Workshop), Vancouver (2018), p: 69 - 78. [doi: 10.1109/IPDPSW.2018.00019]

Architecture Use-Modes

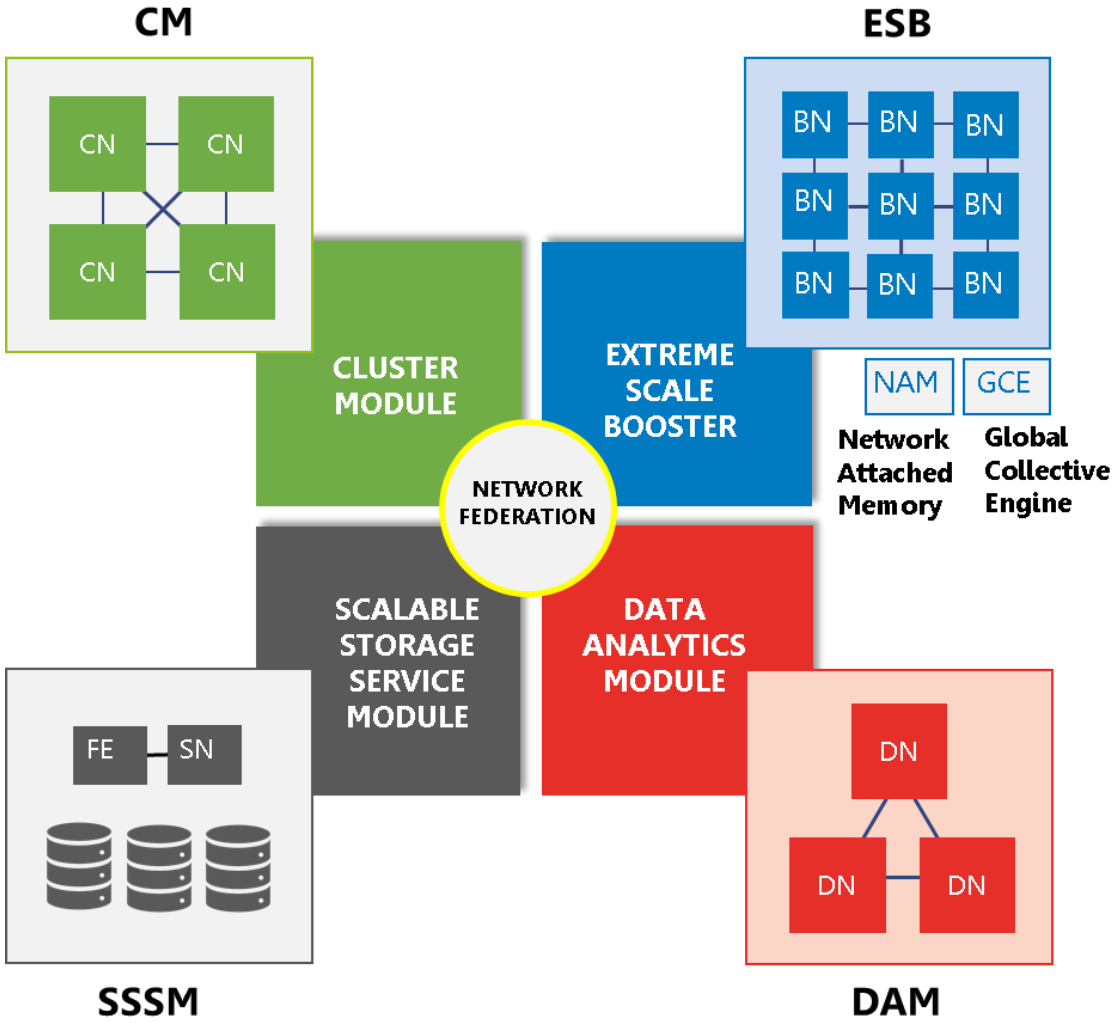


Cluster-Booster use mode

Code partition
Workflow
I/O forward

- **Kreuzer, et al.,** *Application Performance on a Cluster-Booster System.* IPDPSW – HCW (2018) [10.1109/IPDPSW.2018.00019]
- **Kreuzer et al.** *The DEEP-ER project: I/O and resiliency extensions for the Cluster-Booster architecture.* HPCC'18 proceedings (*2018)* [10.1109/HPCC/SmartCity/DSS.2018.00046]
- Wolf et al., *PIC algorithms on DEEP: The iPiC3D case study*. PARS-Mitteilungen 32, 38-48 (2015)
- Christou et al., *EMAC on DEEP*, Geoscientific model devel.(2016) [10.5194/gmd-9-3483-2016]
- Kumbhar et al., *Leveraging a Cluster-Booster Architecture for Brain-Scale Simulations*, Lecture Notes in Computer Science 9697 (2016) [10.1007/978-3-319-41321-1_19]
- Leger et al., *Adapting a Finite-Element Type Solver for Bioelectromagnetics to the DEEP-ER Platform*. ParCo 2015, Advances in Parallel Computing, 27 (2016) [10.3233/978-1-61499-621-7-349]

DEEP-EST prototype



Source: FZJ

Early-Access program in 2020!

Prototype co-designed with Software and Applications

THE DEEP PROJECTS

- **DEEP** (2011 – 2015)
  - Cluster-Booster architecture
- **DEEP-ER** (2013 – 2017)
  - I/O and resiliency
- **DEEP-EST** (2017 – 2021)
  - Modular Supercomputer Architecture

27 partners
EU funding: 30 M€
Budget: 45 M€

www.deep-projects.eu
@DEEPprojects