Update on Address Hashing and Hash Conflicts in Intel Xeon Scalable Processors

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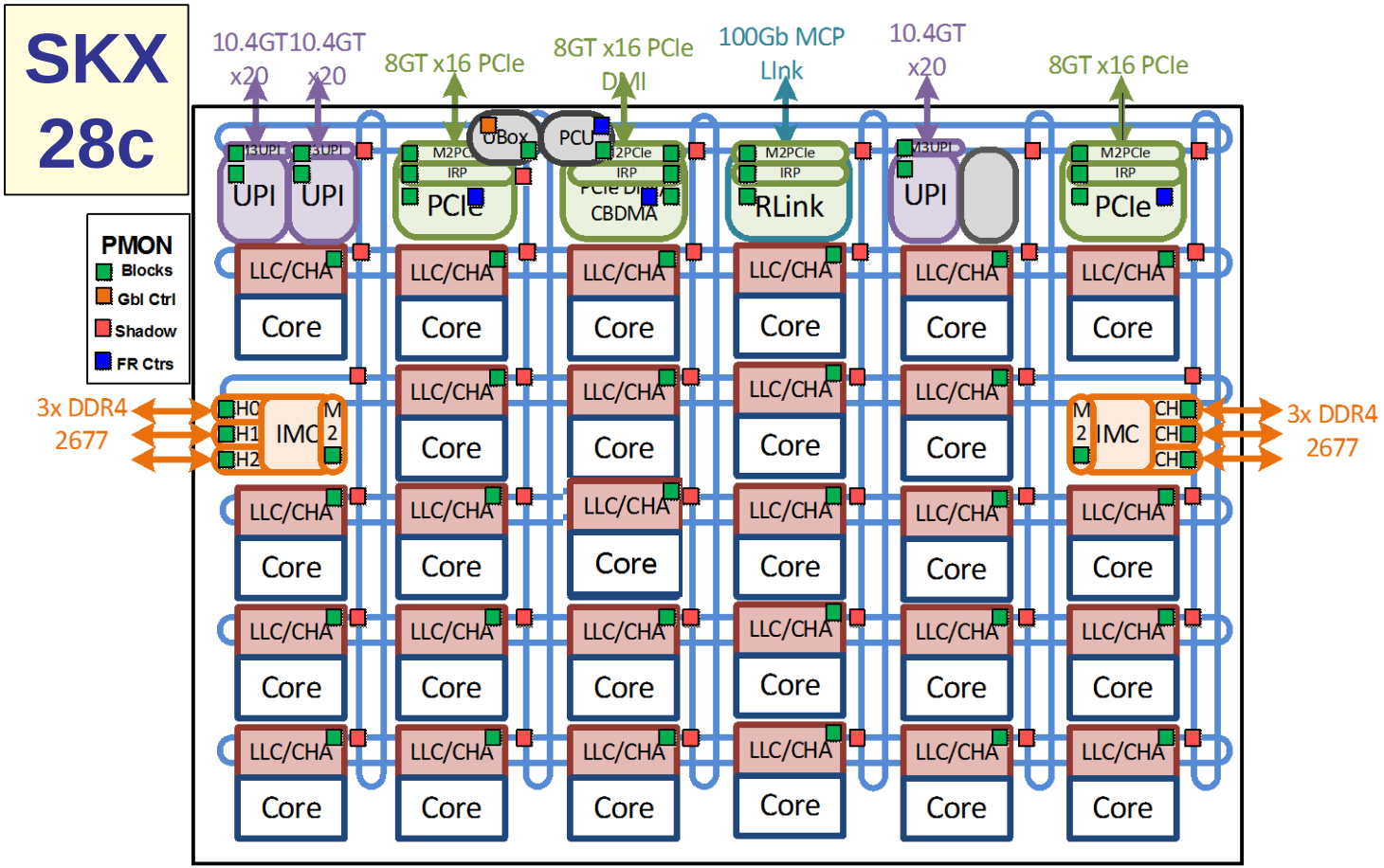
IXPUG BOF SC18

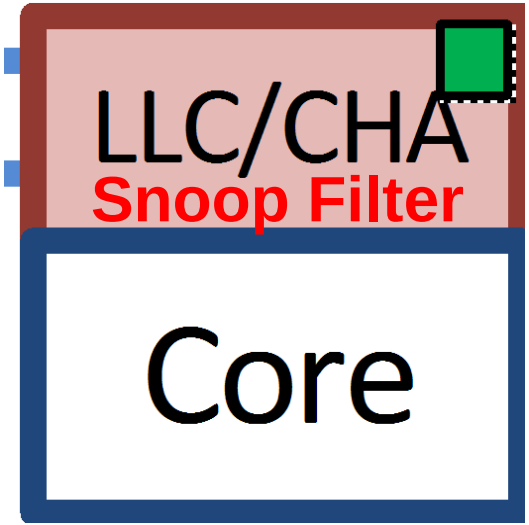


Intel Xeon Scalable Processors:

Each “Core” box includes a core + private L1 and L2 caches

Each cache line address is mapped to exactly one LLC/CHA by an undocumented hash

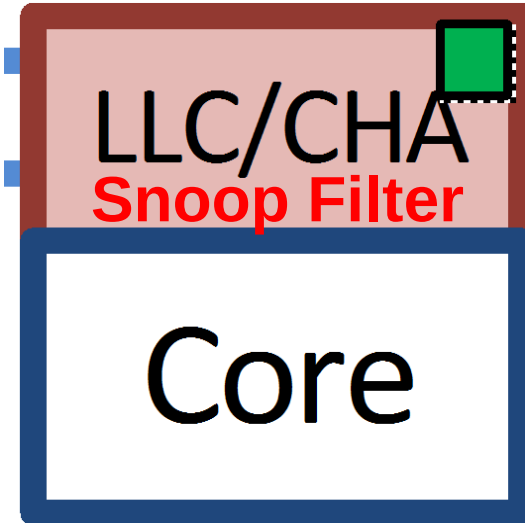
Figure 1-1 from Intel document 336274-001



Cache lines are distributed fairly uniformly ***across*** the LLC/CHA boxes…

But not always uniformly ***within*** each LLC/CHA box

The "**Snoop Filter**" in the LLC/CHA box tracks lines held in L1/L2 caches



When a new Snoop Filter entry is needed, the cache line tracked by the replaced entry must be evicted from all other L1 and L2 caches in the chip

If the line is in active use, it will immediately be reloaded by that other core

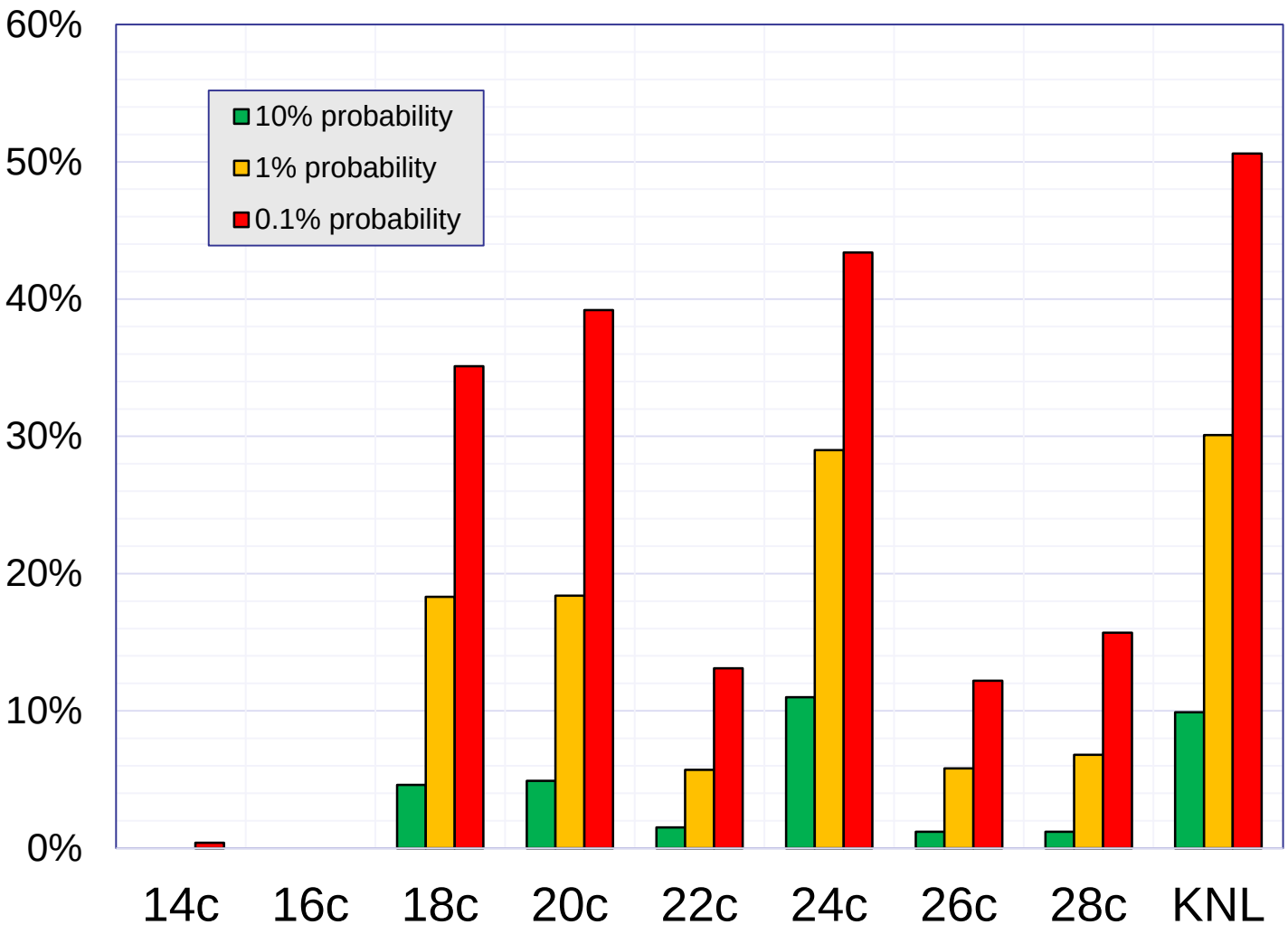
This will cause another line to be evicted, causing another line to be evicted….

Classic case of “thrashing”

Average Snoop Filter Eviction Ratio for repeated array read test on 2 MiB pages

Tests run on:
14c Xeon Gold 6132
16c Xeon Gold 6142
18c Xeon Gold 6150
20c Xeon Gold 6148
22c Xeon Gold 6152
24c Xeon Platinum 8160
26c Xeon Platinum 8170
28c Xeon Platinum 8180
KNL Xeon Phi 7250

Thanks: Dell Customer Solutions Center!



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