INTEL EXTREME PERFORMANCE USERS GROUP

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IXPUG

INTEL EXTREME PERFORMANCE USERS GROUP

- Worldwide organization
- Optimization of scientific applications on Intel based HPC systems
- Now **I**ntel e**X**treme **P**erformance **U**sers **G**roup
  - Originally Intel Xeon Phi Users Group
  - Expanding focus to system hardware beyond the processor, software tools & porgraming models, new workloads (e.g. viz, data analytics, ML)

http://www.ixpug.org/

IXPUG

INTEL EXTREME PERFORMANCE USERS GROUP

- Free exchange of information and ideas
- Meetings and activities open to everyone
- No cost or barrier to participate
- Independent and member run
  - Strong support from, and interactions with, Intel

http://www.ixpug.org/

IXPUG
INTEL EXTREME PERFORMANCE USERS GROUP

Leadership

President: David Martin, Argonne National Laboratory

Vice President: Estela Suarez, Jülich Supercomputing Centre

Secretary: Melyssa Fratkin, Texas Advanced Computing Center

IXPUG Steering Committee

Fabio Affinito
CINECA

Taisuke Boku
University of Tsukuba

Richard Gerber
NERSC/Lawrence Berkeley National Laboratory

Clay Hughes
Sandia National Laboratory

Thomas Steinke
Zuse Institute Berlin

James Lin
Shanghai Jiao Tong University

David Keyes
King Abdullah University of Science & Technology

Kent Milfeld
Texas Advanced Computing Center

Hai Ah Nam
Los Alamos National Laboratory

John Pennycook
Intel

Vit Vondrak
VSB - Technical University of Ostrava

Sergi Siso
STFC Hartree Center

14 major events in 2 years!

SC16 Salt Lake City, Utah | now matters.

Argonne NATIONAL LABORATORY

SC17 Denver, CO | new adventures

TACC

UNIVERSITY OF CAMBRIDGE

ISC High Performance The HPC Event.

IT4Innovations national supercomputing center

CINECA

POLYTECH Peter the Great St.Petersburg Polytechnic University

MGU

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Past Meetings

- IXPUG Annual Meeting, September 12-22, 2016 – Argonne National Laboratory, Argonne, USA
- IXPUG at Intel HPC Developer Conference, November 12-13, 2016 – Salt Lake City, USA
- BoF: “Optimizing Performance on Intel® Xeon Phi and Beyond: Unleashing the Power of Many-Core Processors”, November 16, 2016 – SC16, Salt Lake City, USA
- IXPUG Annual Spring Meeting, April 10-13, 2017, University of Cambridge, Cambridge, UK
- IXPUG Software-Defined Visualization Workshop, May 22-25, 2017 – TACC, Austin, USA
- IXPUG Russia Annual Meeting, June 1-2, 2017 – Russian Academy of Sciences, Moscow, Russia
- BoF: “Achieving Performance on Large-Scale Intel Xeon Phi Knights Landing Systems”, June 19, 2017 – ISC’17, Frankfurt am Main, Germany
- Workshop: "Experiences on Intel Knights Landing at the One Year Mark”, June 22, 2017 – ISC’17, Frankfurt am Main, Germany

Past Meeting (cont)

- IXPUG Sessions, November 11-12, 2017 – Intel HPC Developer Conference, Denver, USA
- IXPUG BoF, November 14, 2017 – SC17, Denver, USA
- IXPUG Workshop, January 31, 2018 – HPC Asia, Tokyo, Japan
- IXPUG Europe Spring Meeting, March 5-7, 2018 – CINECA, Bologna, Italy
- IXPUG Middle East, April 22-25, 2018 – KAUST, Saudi Arabia
- IXPUG Workshop, June 28, 2018 – ISC'18, Frankfurt, Germany
- IXPUG Software-Defined Visualization Workshop, July 1-12, 2018 – Argonne National Laboratory, Argonne, USA
- IXPUG US Fall Meeting, September 25-28, 2018 – Hillsboro, OR, USA

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Upcoming Events

- IXPUG BoF, SC18, November 15, 2018 – Dallas, TX, USA
- Workshop at HPC Asia, January 14, 2019 – Guangzhou, China
- IXPUG Europe Spring Meeting, TBD

IXPUG Working Groups

- Introduced to foster greater collaboration and knowledge-sharing
- Regular (~monthly) teleconferences
  - Attended by IXPUG members and Intel engineers
  - Focused on topics of particular interest to the community
- Open to **anybody** who wishes to join
- Visit https://www.ixpug.org/working-groups for more information
- Mailing lists and discussion forums are live
- Talk to John Pennycook <john.pennycook@intel.com> with ideas

IXPUG Working Groups

Focused on fostering collaborations of cross sharing open standard techniques, best practices, etc.

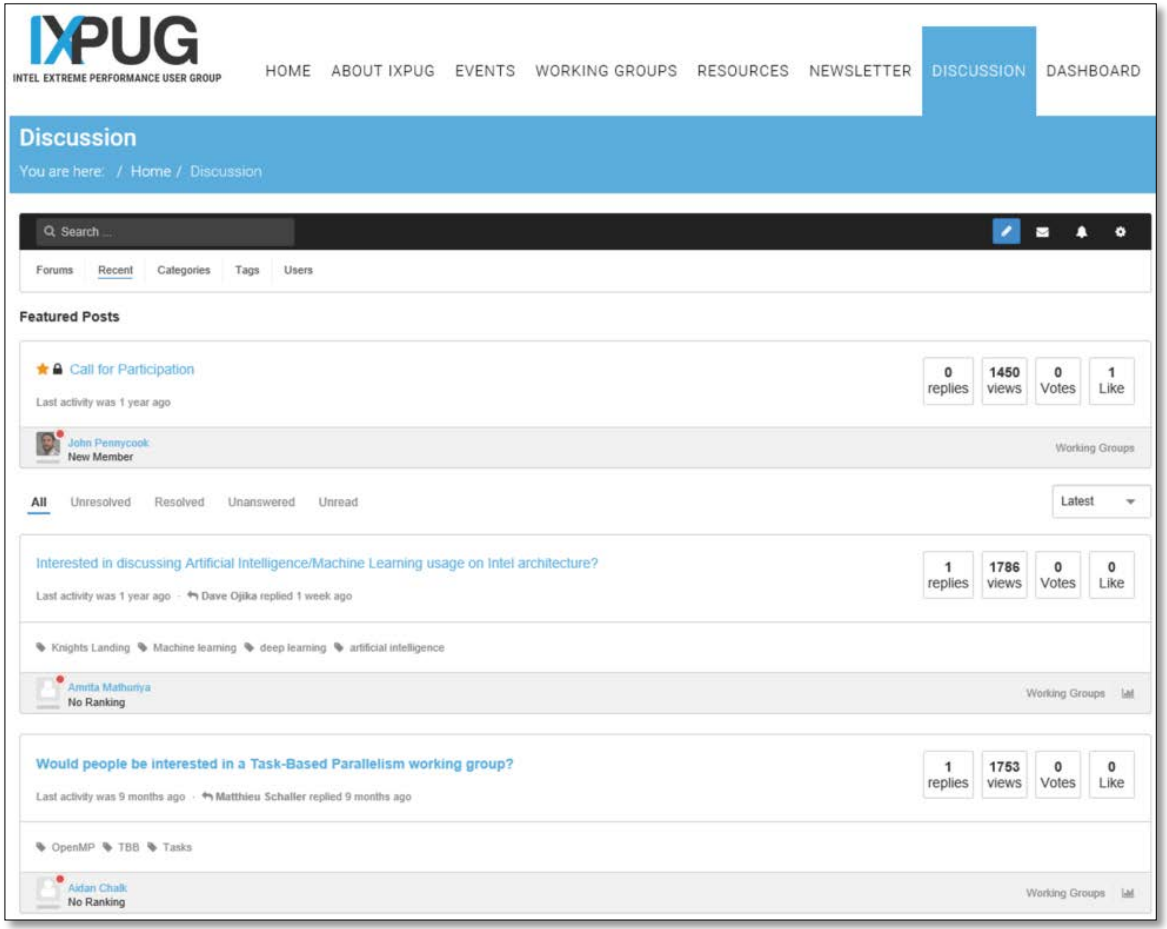
- **Timeline:** ~monthly virtual conferences meetings
- **Attendance:** combination of Intel experts and industry luminaries
- **Cost:** this is a **FREE**, open to the public meeting and all are welcome to join
- **Registration:** https://www.ixpug.org/working-groups for more information
- **Material Location:** all technical presentations and recordings are posted on the website mentioned above

Date	Location	Description
January 11, 2018	Virtual	"**Vectorization of Inclusive/Exclusive Scan in Compiler 19.0**" (Nikolay Panchenko, Intel): We propose a new OpenMP syntax to support inclusive and exclusive scan patterns. In computer science, this pattern is also known as a prefix or cumulative sum. The proposal defines several new constructs to support inclusive and exclusive scans through OpenMP, defines semantics for these constructs and possible combination of parallelization and vectorization. In 18.0 Compiler 3 new OMP SIMD experimental features were added: vectorization of loops with breaks, syntax for compress/expand patterns and syntax for histogram pattern.
February 8. 2018	Virtual	**Threading Building Blocks (TBB) Flow Graph** (*Pablo Reble, Intel*) Expressing and Analyzing Dependencies in Your C++ Application. This session focuses on Flow Graph, an extension to the Threading Building Blocks (TBB) interface that can be used as a coordination layer for heterogeneity that retains optimization opportunities and composes with existing models. This extension assists in expressing complex synchronization and communication patterns and in balancing load between CPUs, GPUs, and FPGAs.
March 8, 2018	Virtual	**"Compiler Prefetching for Knights Landing"** (*Rakesh Krishnaiyer, Intel):* We will cover some of the recent changes in the compiler-based prefetching (for Knights Landing and Skylake) and provide tips on how to tune for performance using compiler prefetching options, pragmas and prefetch intrinsics.
April 12, 2018	Vitual	"**Topology and Cache Coherence in Knights Landing and Skylake Xeon Processors**" () This talk will review some of the most important new features of the coherence protocol (such as "snoop filters", "memory directories", and non-inclusive L3 caches) from a performance analysis perspective. For both of these processor families, the mapping from user-visible information (such as core numbers) to spatial location on the mesh is both undocumented and obscured by low-level renumbering. A methodology is presented that uses microbenchmarks and performance counters to invert this renumbering. This allows the display of spatially relevant performance counter data (such as mesh traffic) in a topologically accurate two-dimensional view.
May 10, 2018	Virtual	**"High Productivity Languages"** (*Rollin Thomas, NERSC and Sergey Maidanov, Intel*): The challenges of numerical analysis and simulations at scale use tools such as Python which are often used for prototyping are not designed to scale to large problems. Therefore, new approaches are required for address scalability and productivity aspects of applied science that combines two distinct worlds, the best of HPC and database worlds.

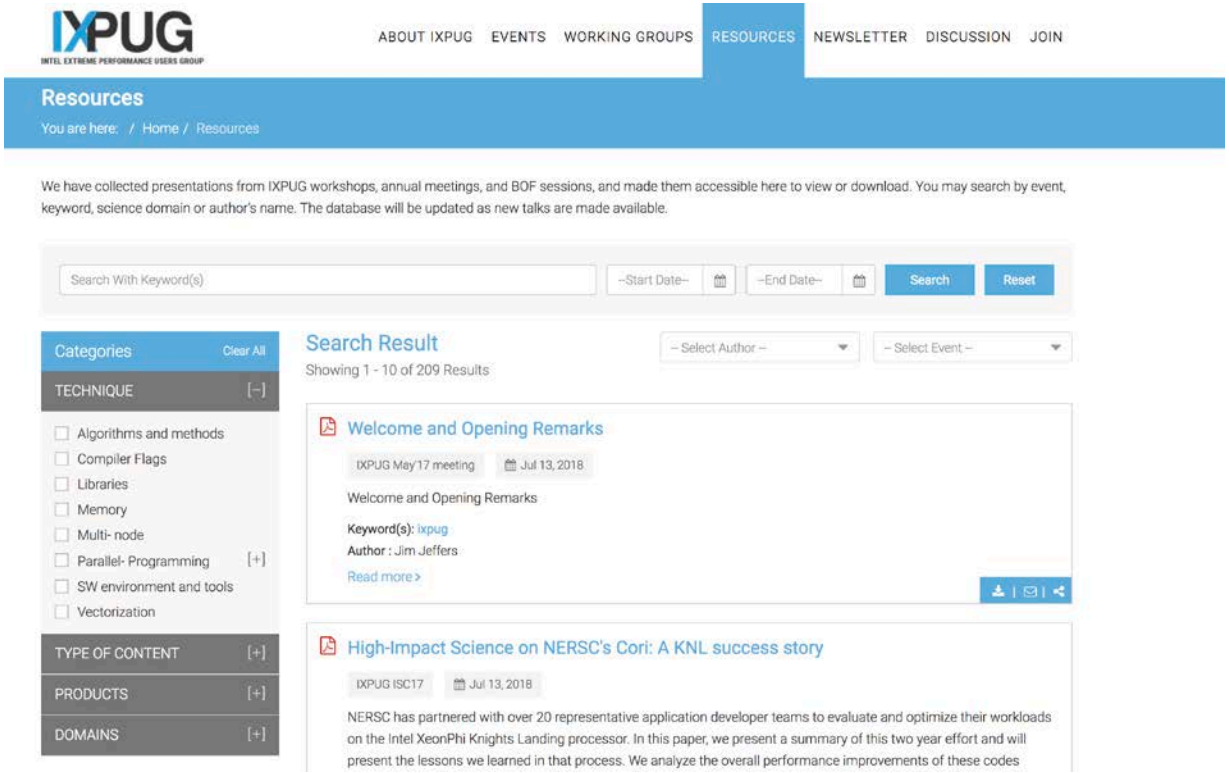
IXPUG Discussion Forums

Focused on building a community that supports open discussions that address questions, technique suggestions, etc. on general purpose Intel architecture using open standards

- Start a discussion thread
- Share your learnings and experiences
- Encourage others to join
- Visit https://www.ixpug.org/discussion



IXPUG Resources



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How to Get Involved

- Join IXPUG (www.ixpug.org)
- Connect with us on Twitter @IXPUG1
- Contribute to an IXPUG Forum
- Participate in an IXPUG Working Group
- Attend an IXPUG Event
- Volunteer for the Program Committee for an IXPUG Event
- Submit Your Work to an IXPUG Event
- Host an IXPUG Event
- Volunteer for the IXPUG Steering Group

IXPUG Elections

- Positions: President, Vice President, Secretary
- 2-year Term, starting January 1, 2019
- We are seeking nominations by October 1
- Voting will take place in November
- New officers will be announced by end of year
- *If you would like to nominate someone (or yourself) for one of the officer positions, please contact Melyssa Fratkin, IXPUG Secretary – mfratkin@tacc.utexas.edu*

Officer Descriptions

- **President**: Coordinates IXPUG meetings and activities. Leads and represents IXPUG at meetings and in the community. Ensures that IXPUG activities adhere to charter policies and protocol.
- **Vice President**: Performs the functions of the president when president is not in attendance at meetings, or when specific duties are delegated to the VP.
- **Secretary**: Manages IXPUG documents and manages the web site. Assures that documents are archived in a location accessible to members and the public. The secretary is also responsible for IXPUG correspondence and reports as well as managing elections.
- Officers will be elected to serve two-year terms, which may be extended to three years by a majority vote of the Steering Committee. If the President is unable or does not fulfill the presidential duties, or resigns, the Vice-President will assume the presidential duties and complete the President's term. A vacancy of the Vice-President or Secretary will be filled by a majority vote of the Steering Committee.

OPUG

The Omni-Path Users Group is an independent users group that provides a forum for the free exchange of information and ideas that enhance the usability and efficiency of scientific applications running on large High Performance Computing (HPC) systems using the Intel Omni-Path Architecture fabric. Participation in OPUG meetings and other activities is open to anyone interested in using OPA Fabric for large-scale scientific or technical computing.

For more information, see https://www.psc.edu/user-resources/computing/omni-path-user-group